REMARKS / ARGUMENTS

Claims 1-4 remain pending in this application. Claims 5-31 have been canceled without prejudice or disclaimer.

35 U.S.C. §103

Claims 1-4 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Nishizawa et al (U.S. Pub. No. 2002/0030270). The rejection is traversed as follows.

As previously argued, the signal interconnection between pads (11A, 11B) of a control chip (10) and pads (21A, 21B) of memory chip (20) is controlled by control chip (10). The signal interconnection is achieved via a first bonding wire (16, which is a relatively short wire) connecting pads (11A, 11B) of control chip (10) with the inner lead of the first lead (2c, 2d) and third bonding wire (16, which is a relatively long wire) connecting the inner lead of the first lead (2c, 2d) with pads (21A, 21B) of memory chip (20). Therefore, according to the present invention, signal interconnection between the control chip and the memory chip can be achieved by selecting a single lead from among the plurality of leads from the lead frame. As such, special types of lead-frames and/or a special class of control chip having extra bonding pads is not necessary. As such, the overall cost of the package is reduced.

Nishizawa et al do not disclose a third bonding wire connecting the third pad of the second chip to the first lead bonded to the first wire. In other words, Nishizawa et al do not disclose or suggest that the first lead is connected to both the first and third bonding wires.

Applicants believe that the Examiner is interpreting Nishizawa by considering only a sectional view (for example Figures 18 and 19). In the plan view, wires (8) are bonded to signal pads of the first chip (20) and wires (8) are bonded to the signal pads of the second chip (30), and are not commonly bonded to the same lead (7). This lead, for which pads for both first and second chips (20, 30) are commonly connected is a power supply lead (6B: Vss), and is not a signal lead (see Figure 2 and corresponding description of Nishizawa et al).

Furthermore, Figures 18 and 19 of Nishizawa et al merely disclose a package having a combination of a DRAM as a memory and a controller that executes image processing. These figures show an example of a package containing a combination of a DRAM and a flash memory, but neither disclose nor suggest that wires (8) that are bonded to signal pads of the first chip (20) and wires (8) are bonded to the signal pads of the second chip (30) and are also commonly bonded to the same lead (7). In fact, the lead that is contacted to the wire bonded to the pad of the DRAM chip and the lead contacted to the wire bonded to the pad of the controller are different from one another (see Figures 18 and 19 which show a compartment line in the

sectional view of the lead). As such, applicants strongly maintain that the pending claims patentably define the present invention over the cited art.

Request for an Interview

Applicants once again request that the Examiner contact the undersigned in order to expedite prosecution of this application.

Conclusion

In view of the foregoing, Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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